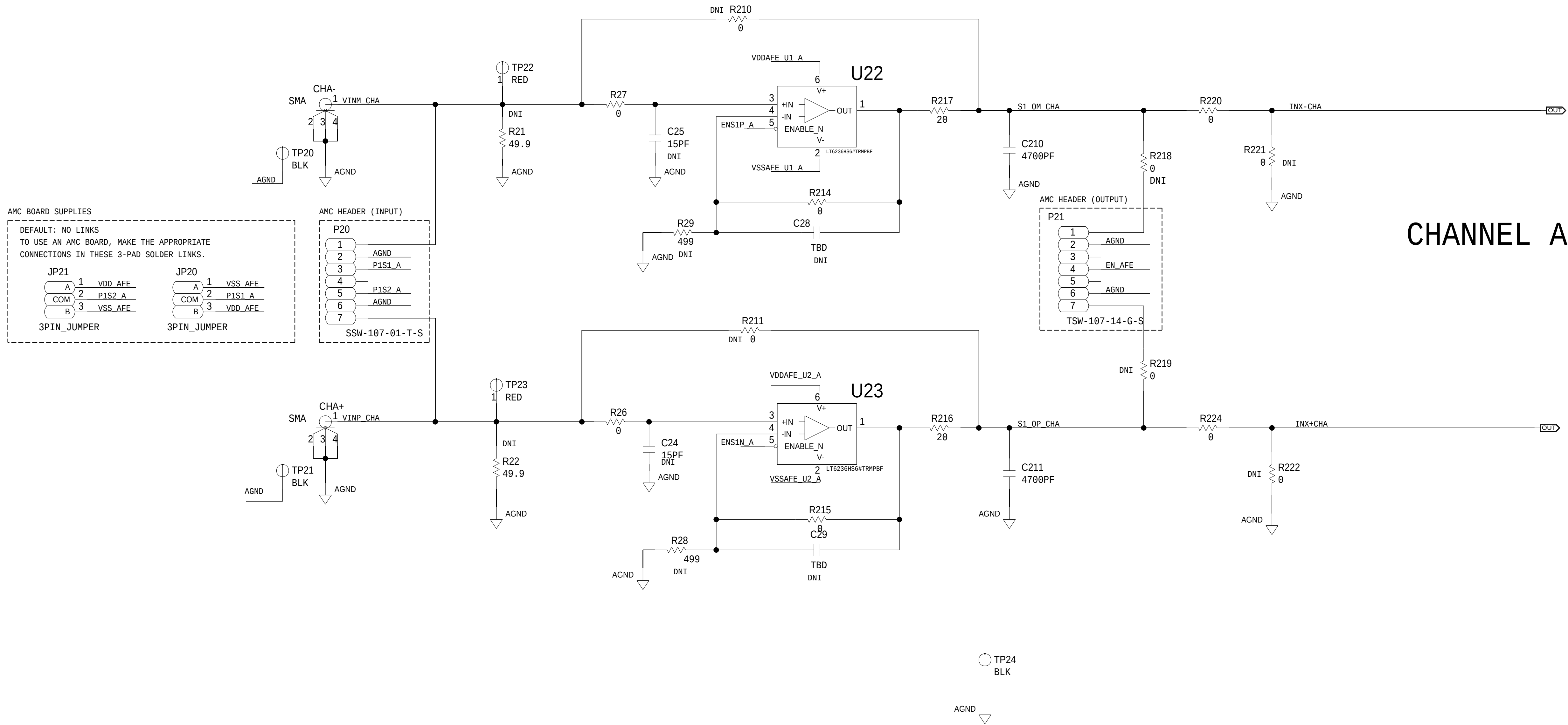


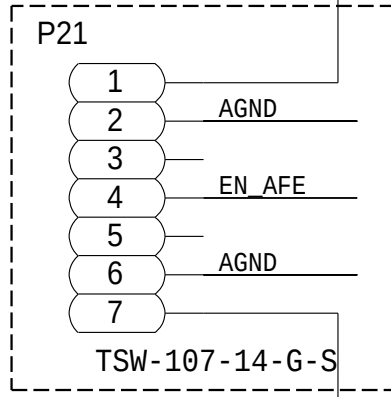
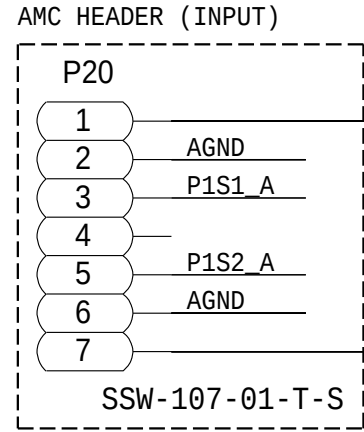
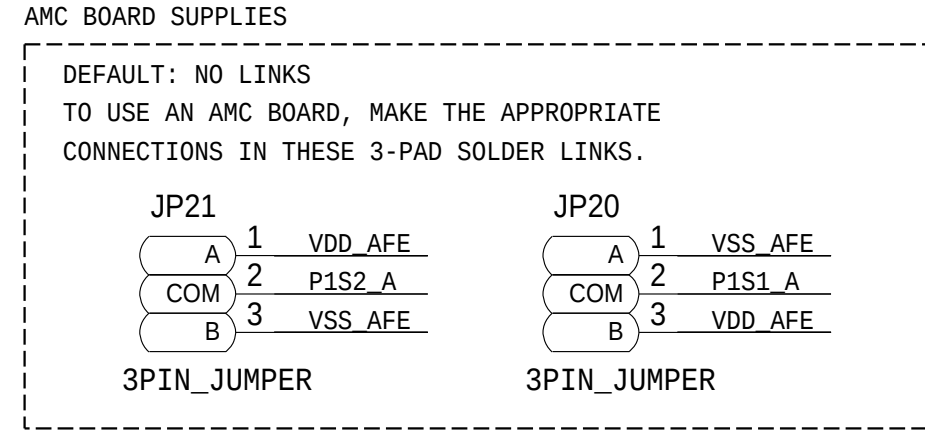
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PRECISION SIGNAL CONDITIONING CIRCUITS
CHANNEL A

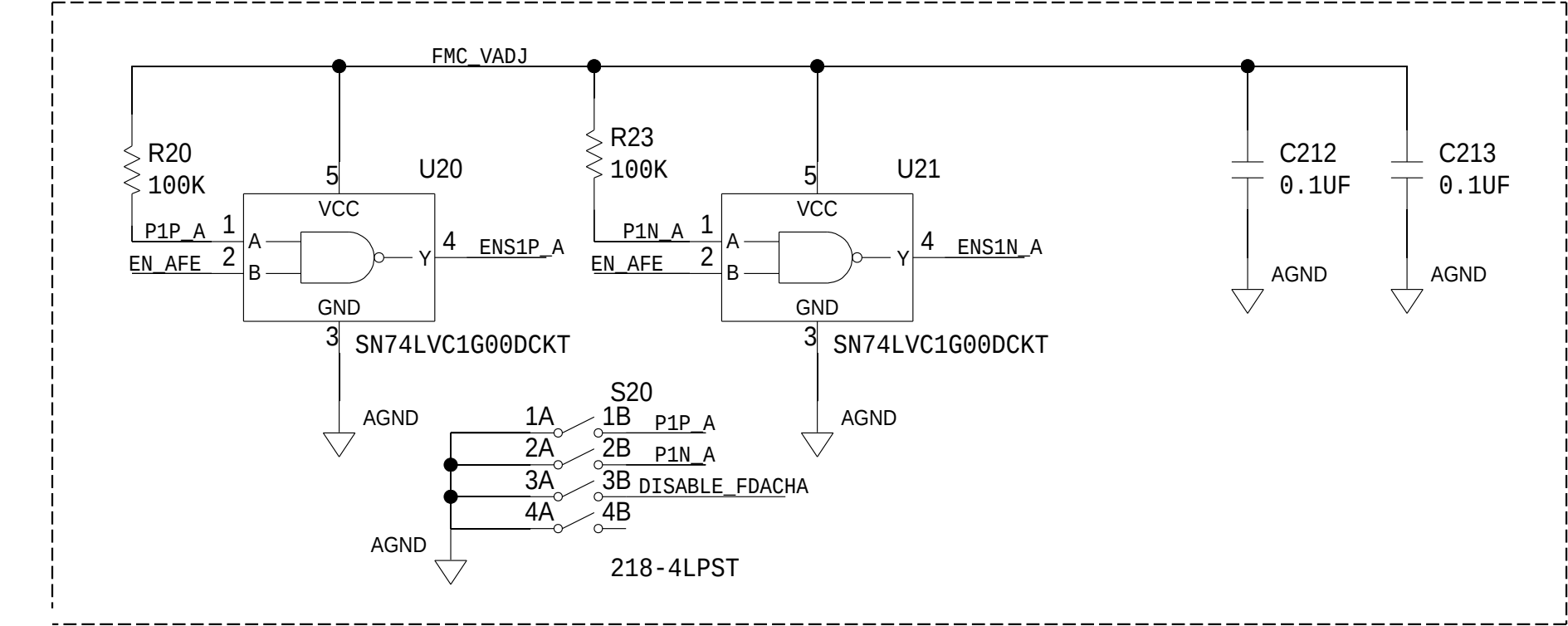
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REV	DESCRIPTION	DATE	APPROVED



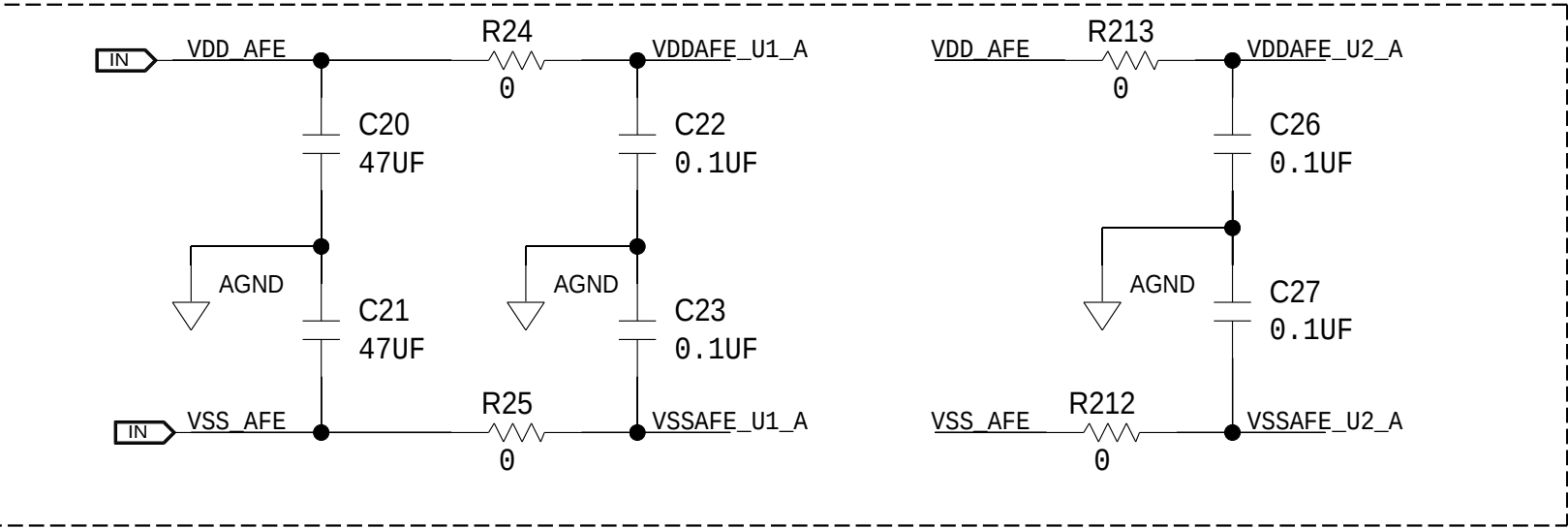
CHANNEL A ANALOG INPUTS



AMPLIFIER DISABLE LOGIC



STAGE 1 SUPPLY DECOUPLING



SCHEMATIC

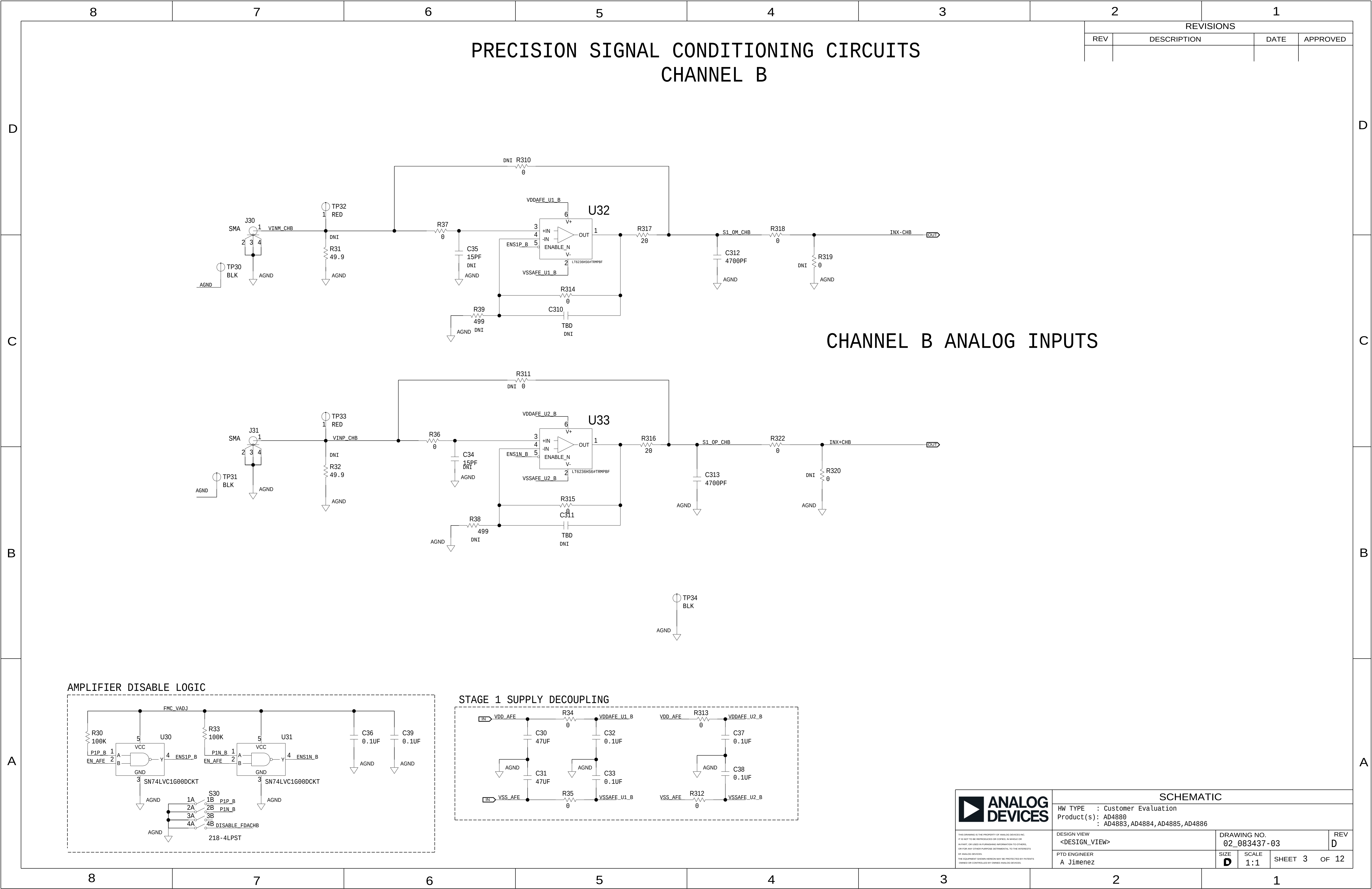
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Product(s) : AD4880
: AD4883, AD4884, AD4885, AD4886

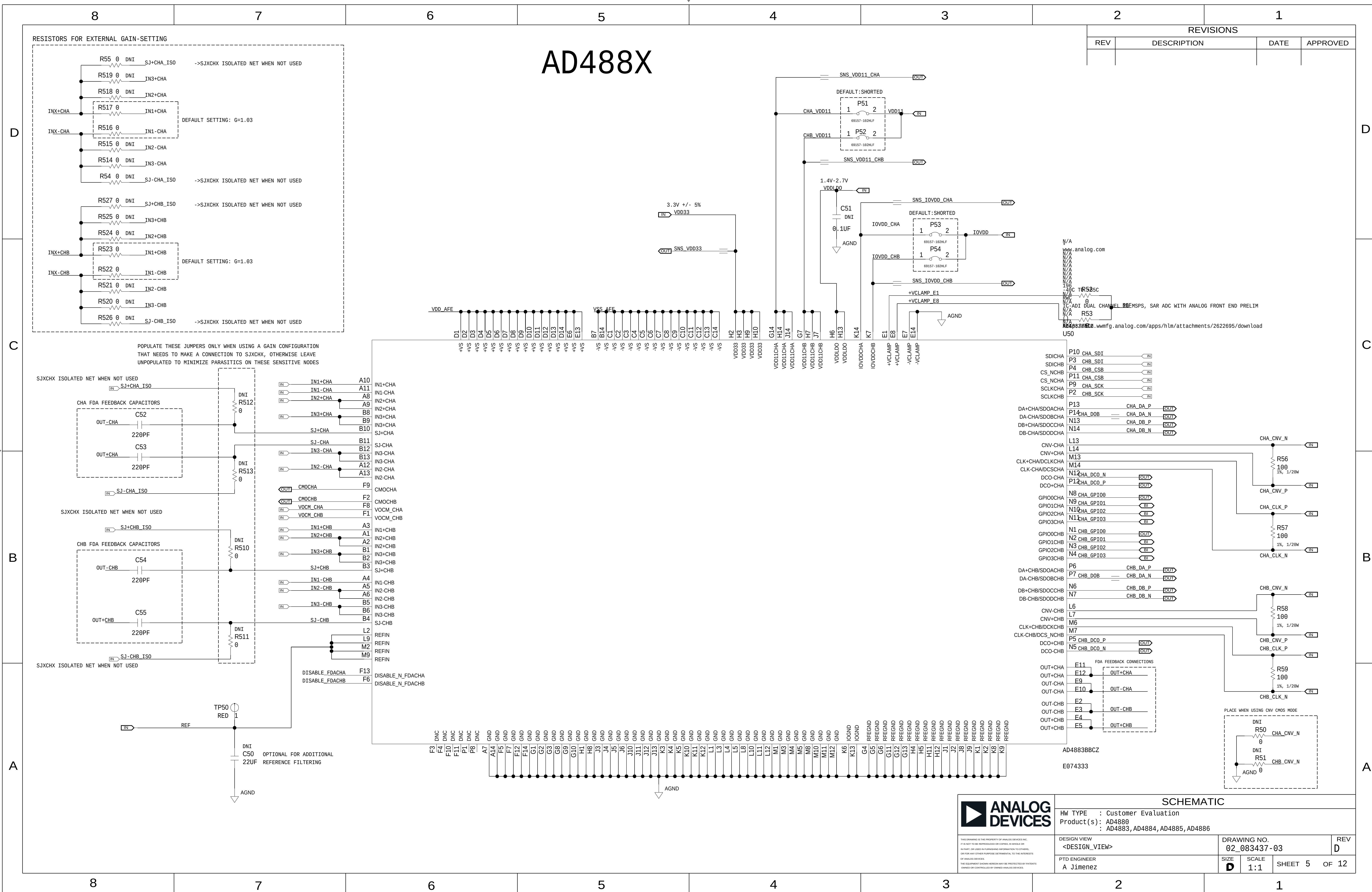
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PTD ENGINEER
A Jimenez

DRAWING NO.
02_083437-03

REV
D

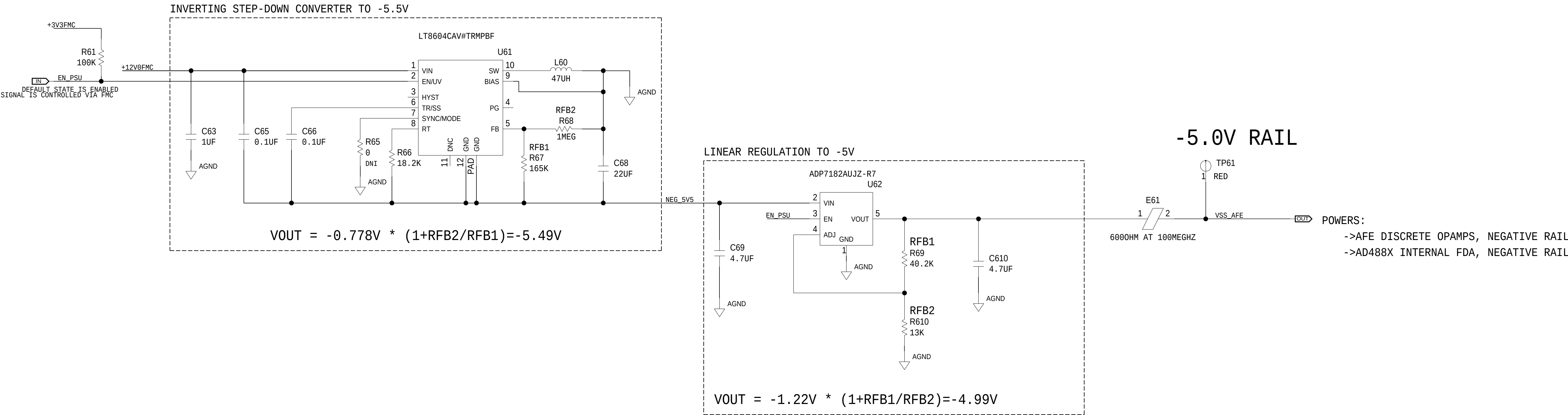
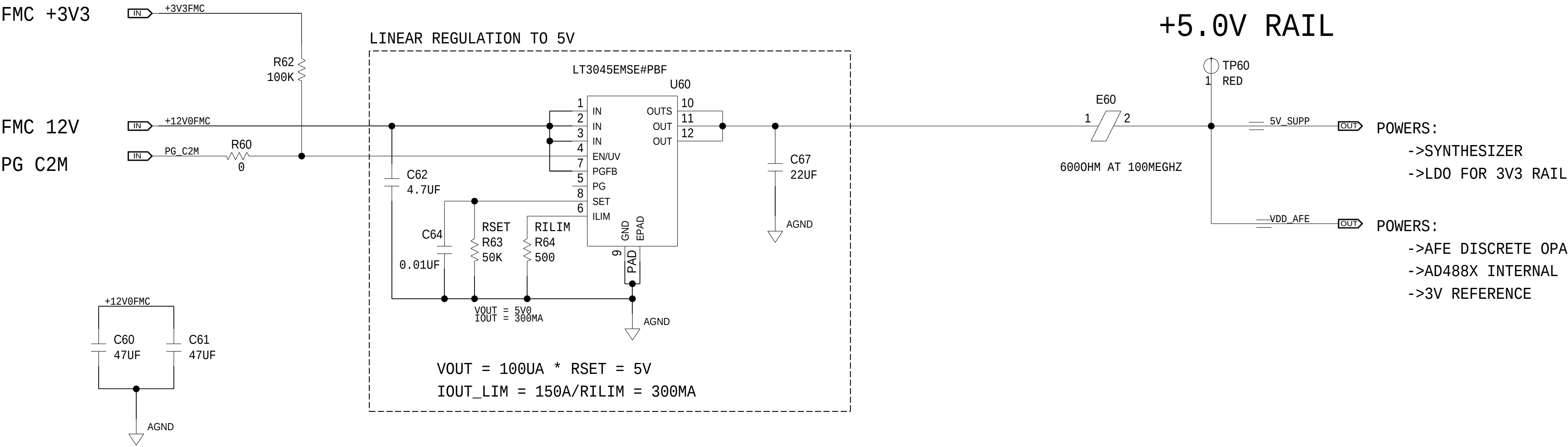
SIZE D SCALE 1:1 SHEET 2 OF 12





REFERENCE & AMPLIFIER SUPPLY GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

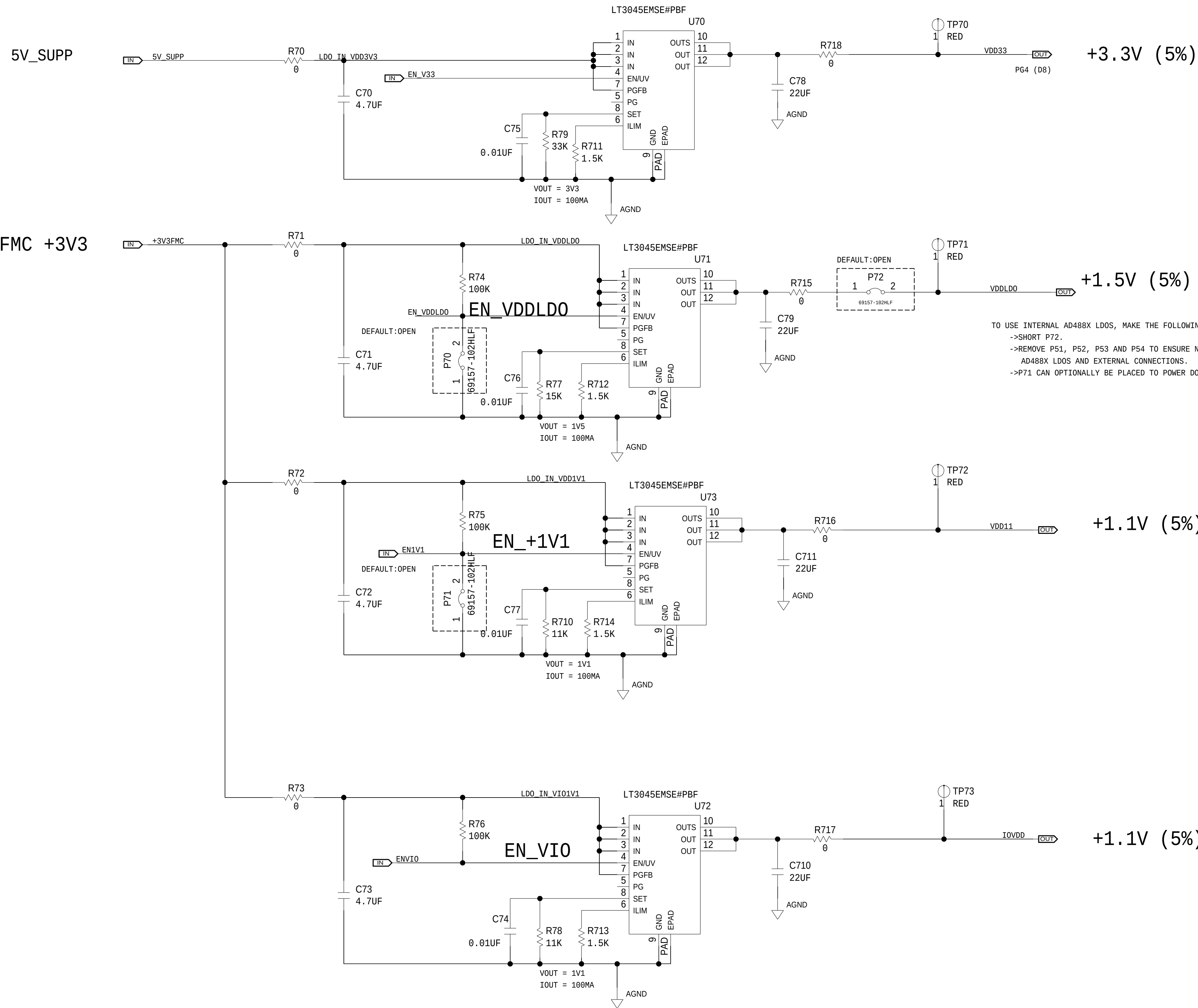


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SCHEMATIC				
HW TYPE : Customer Evaluation				
Product(s): AD4880				
: AD4883, AD4884, AD4885, AD4886				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-03		REV D	
PTD ENGINEER A Jimenez	SIZE D	SCALE 1:1	SHEET 6	OF 12

AD488X DEVICE POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): AD4880 : AD4883, AD4884, AD4885, AD4886			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-03	REV D	
PTD ENGINEER A Jimenez	SIZE D	SCALE 1:1	SHEET 7 OF 12

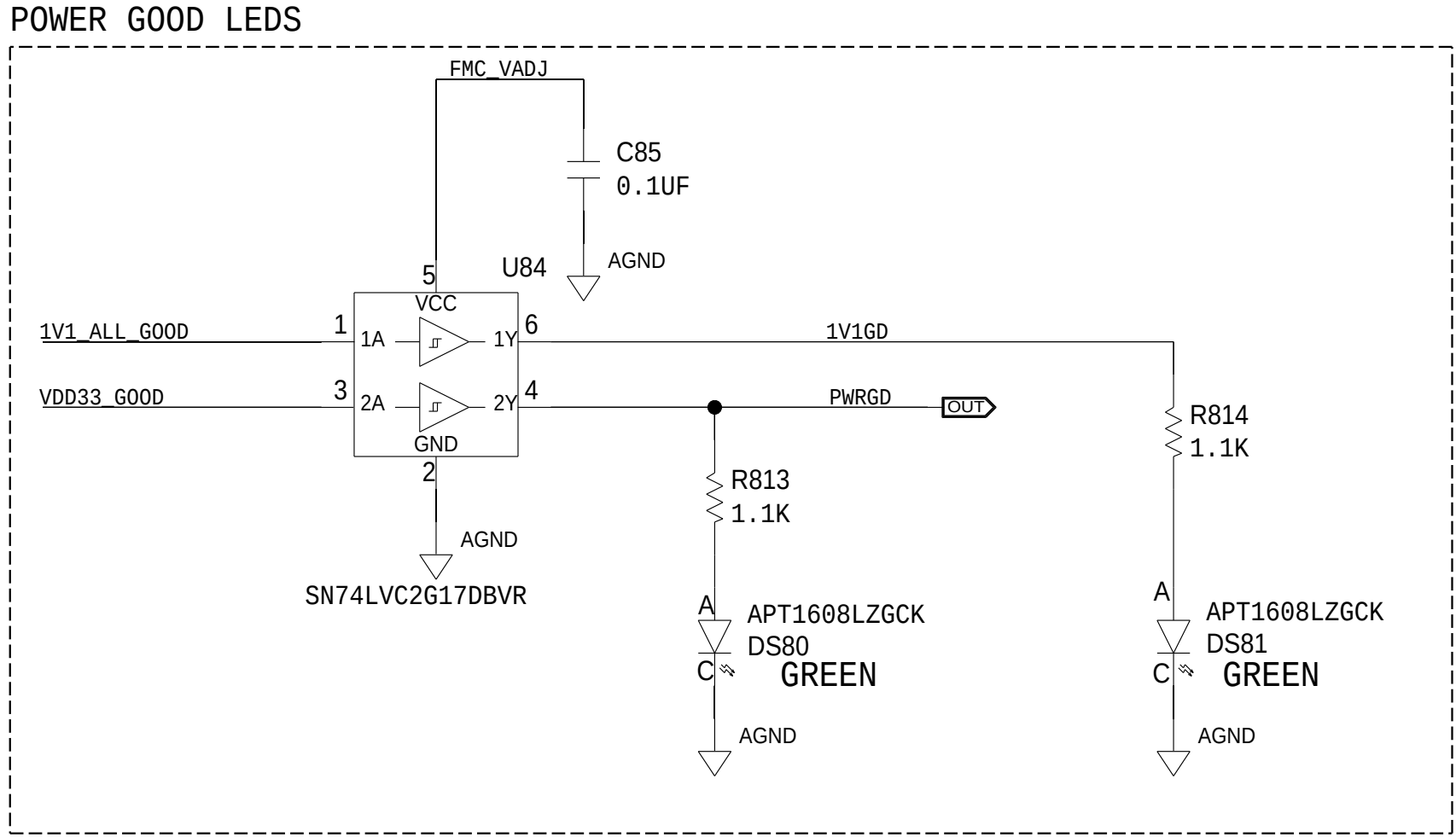
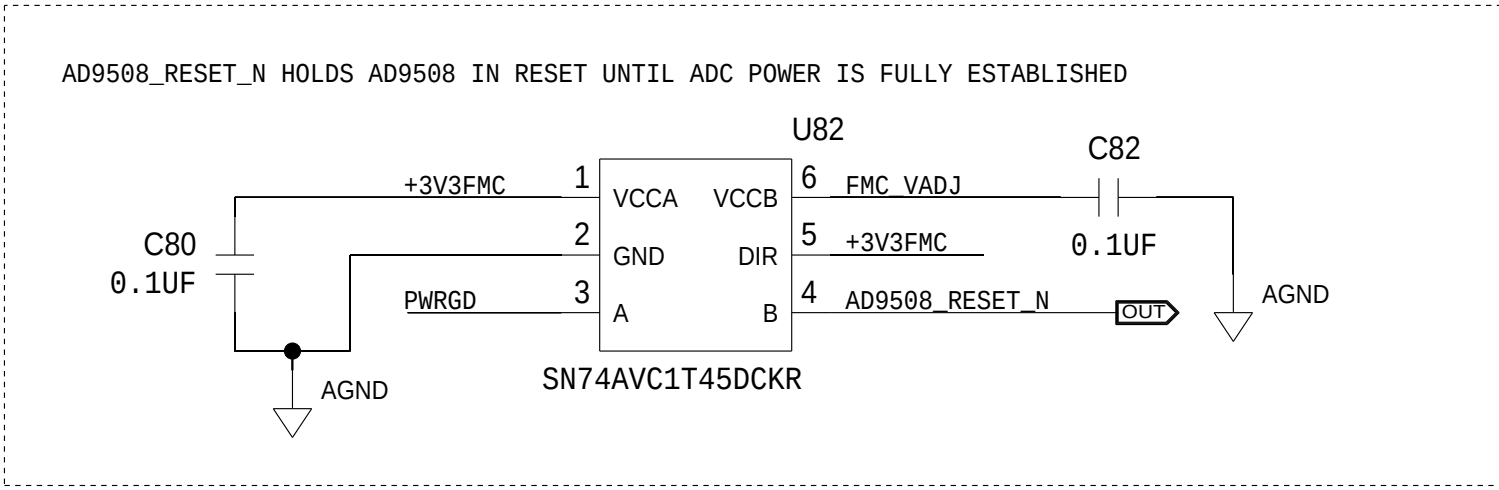
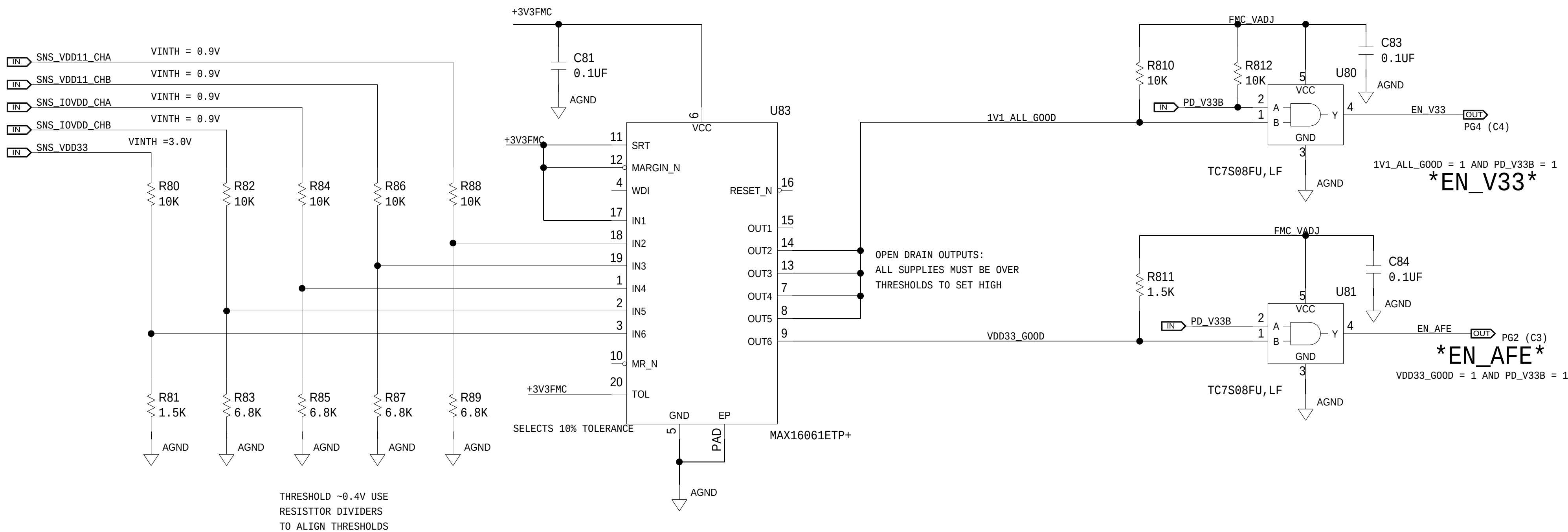
SUPPLY SEQUENCE CIRCUITS

12V FMC WILL POWER +5V0 AND -5V0 RAILS, SWITCHER STARTUP DELAYS -5V0 WRT +5V0
PG_C2M WILL ENABLE 5V0 LDO IC. EN_PSU ENABLES -5V0 LDO.BOTH SIGNALS HAVE PULL UPS TO DEFAULT ON

3V3 FMC WILL PROVIDE POWER FOR OPTIONAL AD488X 1V5 LDO SUPPLY
5V0 WILL PROVIDE SUPPLY FOR AD488X 3V3 LDO
3V3 FMC SUPPLY WILL PROVIDE SUPPLY FOR ALL 1V1 LDO ICS
LDO ICS CONTROL SIGNALS ALL HAVE PULL UPS:

EN_VDDLDO HAS PU AND JUMPER OPTION TO DISABLE
EN_1V1 HAS PU (NO OTHER INPUT CONNECTION)
EN_VIO HAS PU (NO OTHER INPUT CONNECTION)

AD488X IOVDD, VDD11 WILL POWER UP
AD488X VDD11 VOLTAGE WILL BE SENSED, VIO WILL BE SENSED
IF PG_2CM IS NOT PULLED LOW AT FMC AND BOTH THESE VOLTAGES PRESENT
THE AD488X'S 3V3 SUPPLY WILL BE ENABLED WITH THE EN_V33 SIGNAL
PD_V33B ALLOWS THIS EN_V33 TO BE OVERRIDDEN VIA THE FMC (PU ENSURES DEFAULT TO NOT OVERRIDE)
ONCE THE AD488X'S 3V3 HAS BEEN ESTABLISHED, EN_AFE WILL ENABLE THE REFERENCE AND THE
ANALOG FRONT-END OPAMPS (THESE CAN BE OVERRIDDEN VIA PIANO SWITCHES S20, S30)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ANALOG DEVICES		SCHEMATIC	
HW TYPE : Customer Evaluation		Product(s) : AD4880	
		: AD4883, AD4884, AD4885, AD4886	
DESIGN VIEW	<DESIGN_VIEW>	DRAWING NO.	REV
PTD ENGINEER	A Jimenez	02_083437-03	D
SIZE	SCALE	SHEET	OF
D	1:1	8	12

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

+3.3V VCC0

LOOP BW = 62.5KHZ, PM = 51DEG

ADF4350 BCPZ

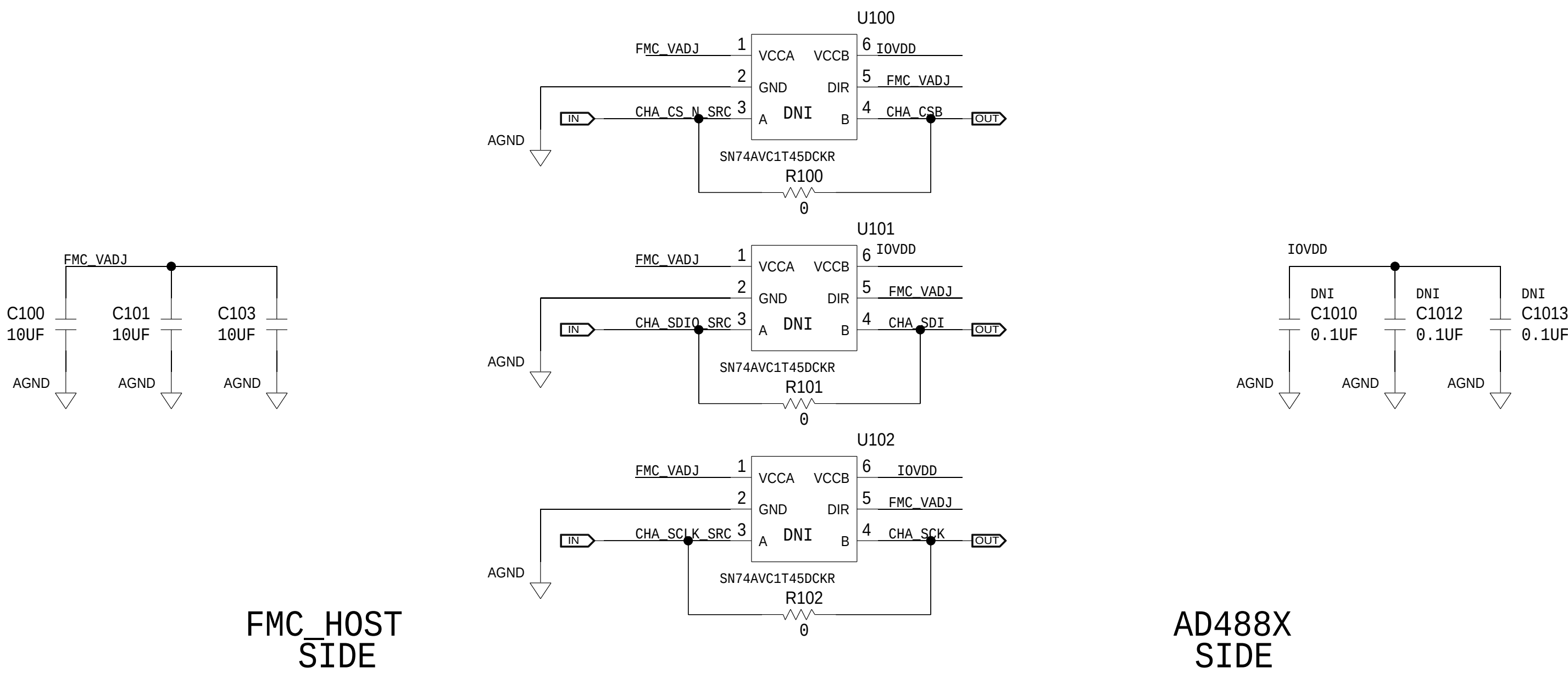
ADF435X LOCK
CONFIGURE MUXOUT FOR DIGITAL LOCK ONLY

PROG_SEL INTENTIONAL NC. ENABLES SPI CONFIG MODE.
 IN_SEL TIED TO SUPPLY. ENABLES DIFFERENTIAL INPUT CLOCK MODE
 S4,S5 PHYSICALLY LEFT FLOATING.
 AD9508_RESET_N IS DERIVED FROM PSU SEQ OUTPUT (PORB).
 LVDS TERMINATION PLACEMENT AT LOAD

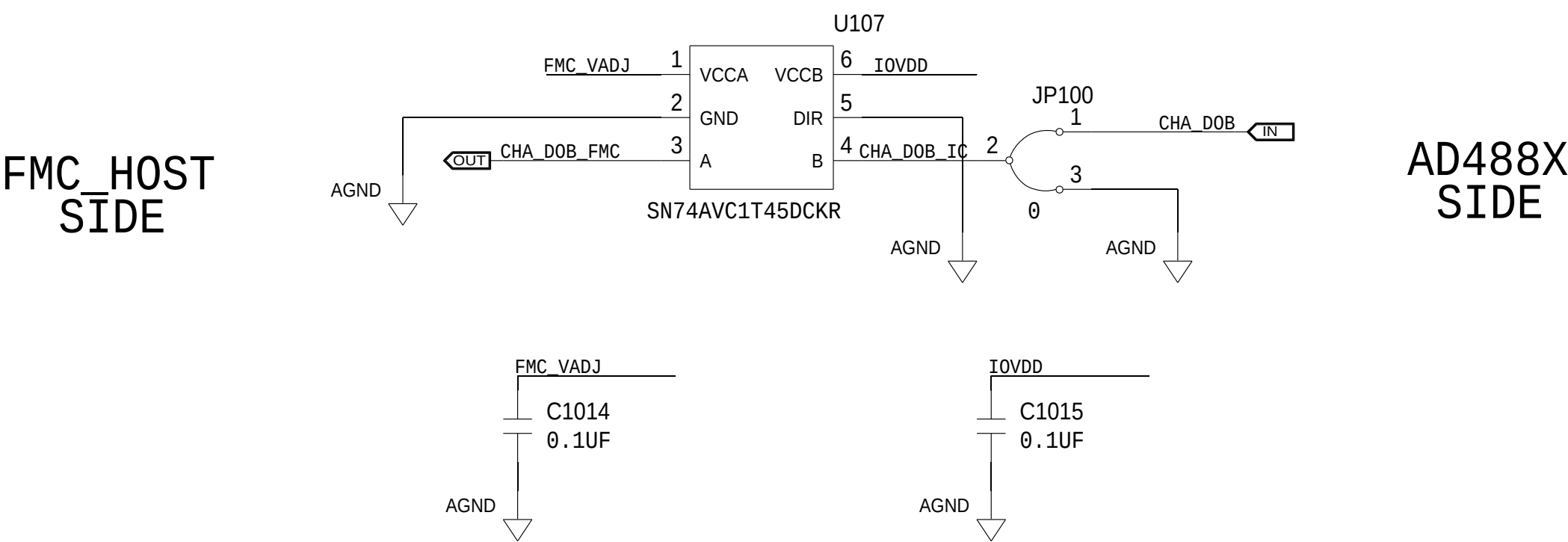
- 1) PROG_SEL INTENTIONAL NC. ENABLES SPI CONFIG MODE.
- 2) IN_SEL TIED TO SUPPLY. ENABLES DIFFERENTIAL INPUT CLOCK MODE
- 3) S4,S5 PHYSICALLY LEFT FLOATING.
- 4) AD9508_RESET_N IS DERIVED FROM PSU SEQ OUTPUT (PORB).
- 5) LVDS TERMINATION PLACEMENT AT LOAD

LEVEL TRANSLATION CH_A

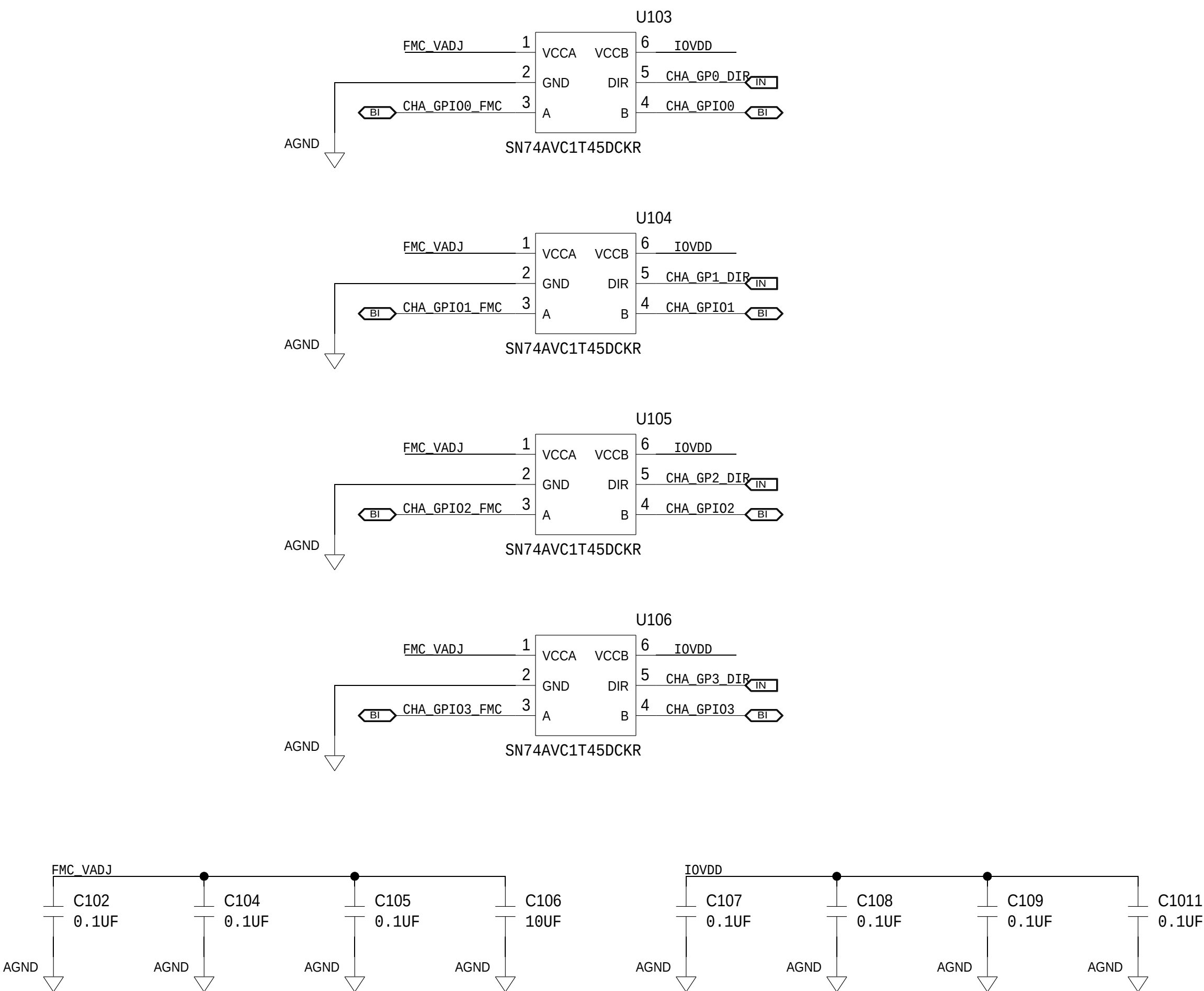
CONFIGURATION SPI LEVEL TRANSLATORS
(NOT INSTALLED BY DEFAULT)



DATA SPI LEVEL TRANSLATORS



GPIO LEVEL TRANSLATORS



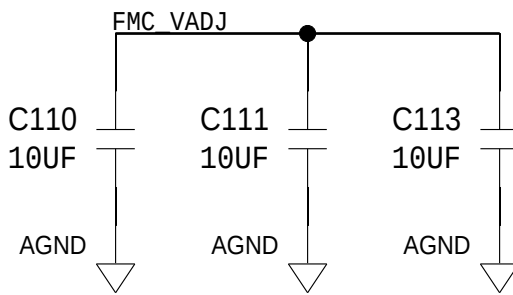
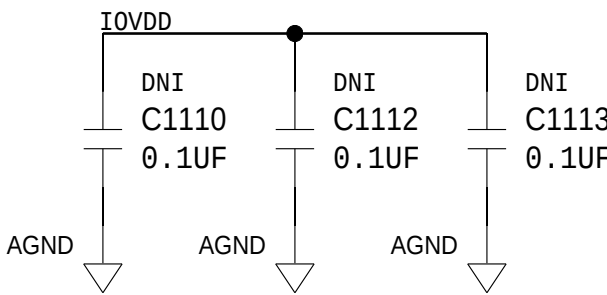
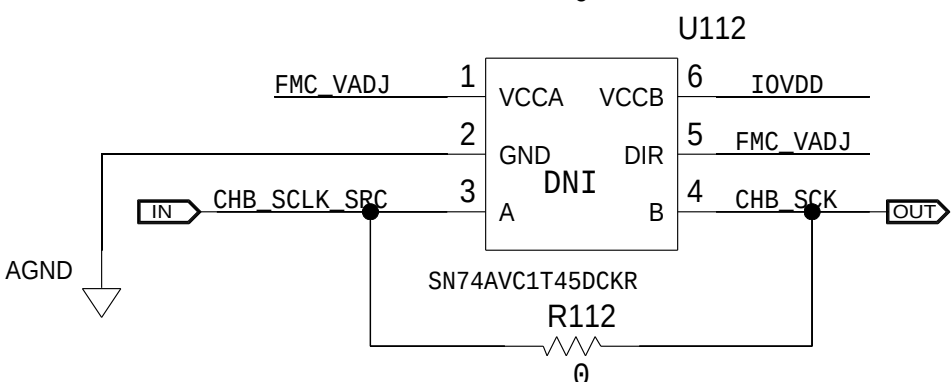
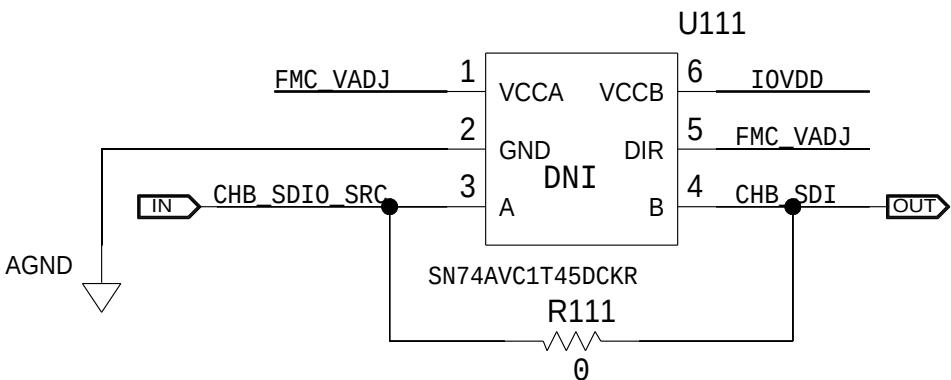
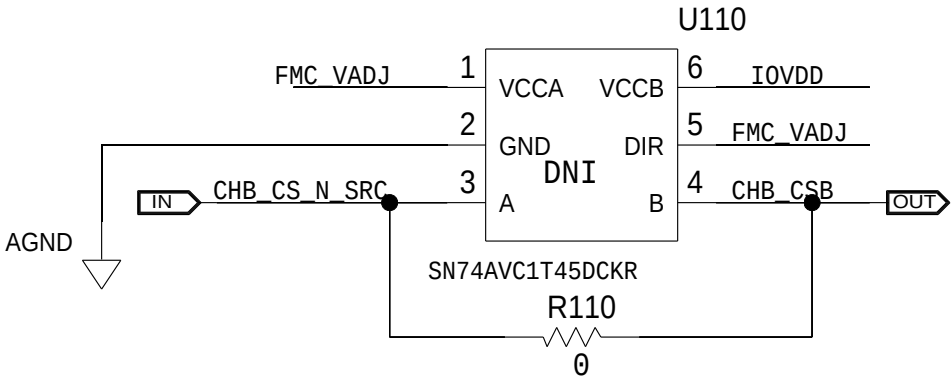
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SCHEMATIC				
HW TYPE : Customer Evaluation Product(s): AD4880 : AD4883, AD4884, AD4885, AD4886				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02_083437-03	
PTD ENGINEER A Jimenez			SIZE D	SCALE 1:1
			SHEET 10	OF 12

LEVEL TRANSLATION CH_B

CONFIGURATION SPI LEVEL TRANSLATORS

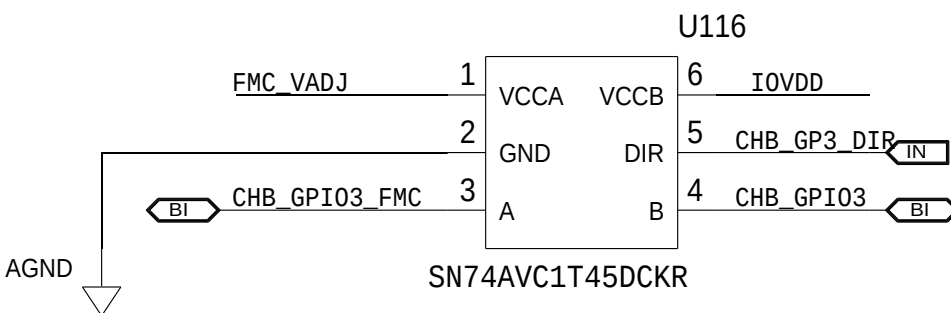
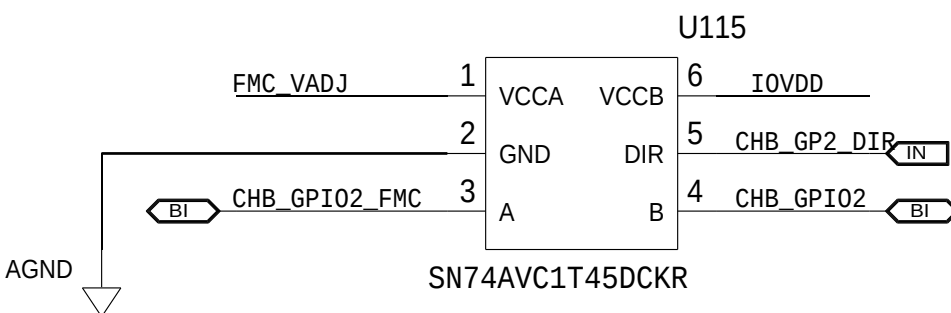
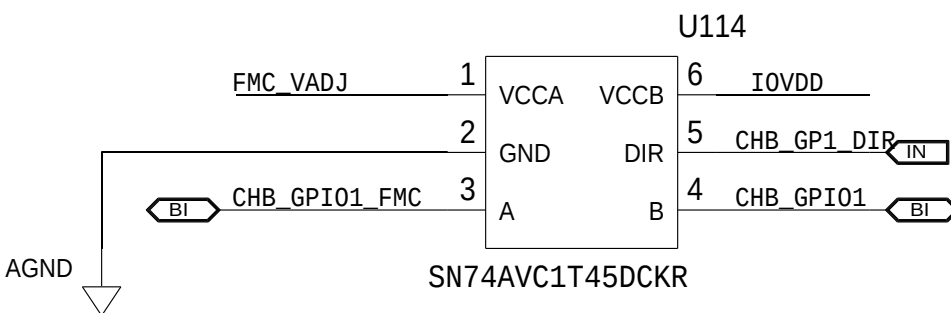
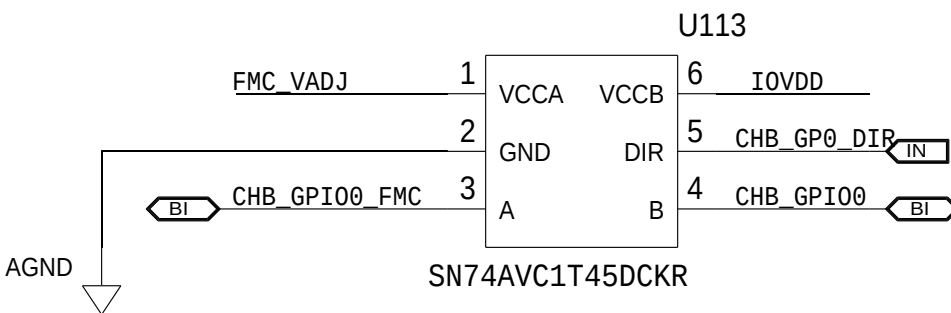
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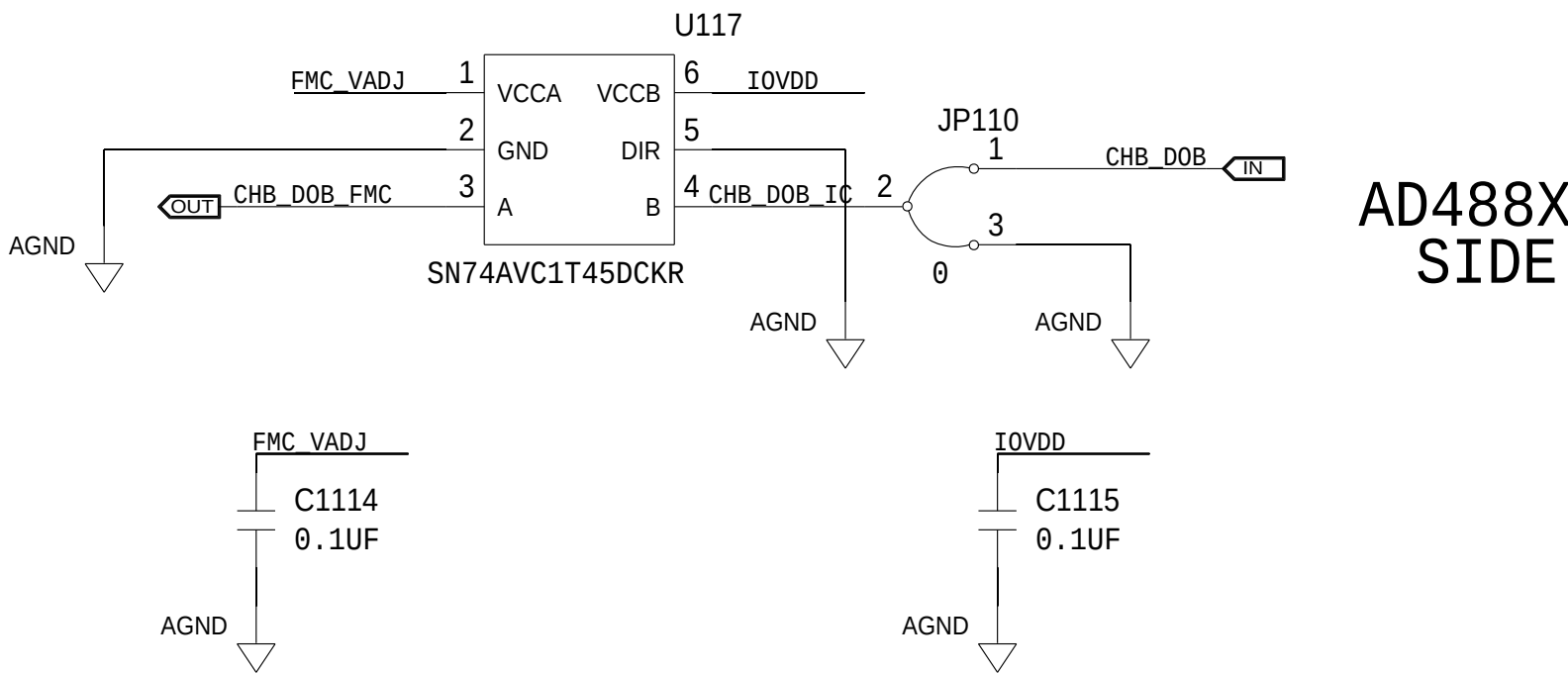
AD488X
SIDE

FMC_HOST
SIDE

GPIO LEVEL TRANSLATORS



DATA SPI LEVEL TRANSLATORS



AD488X
SIDE

FMC_HOST
SIDE

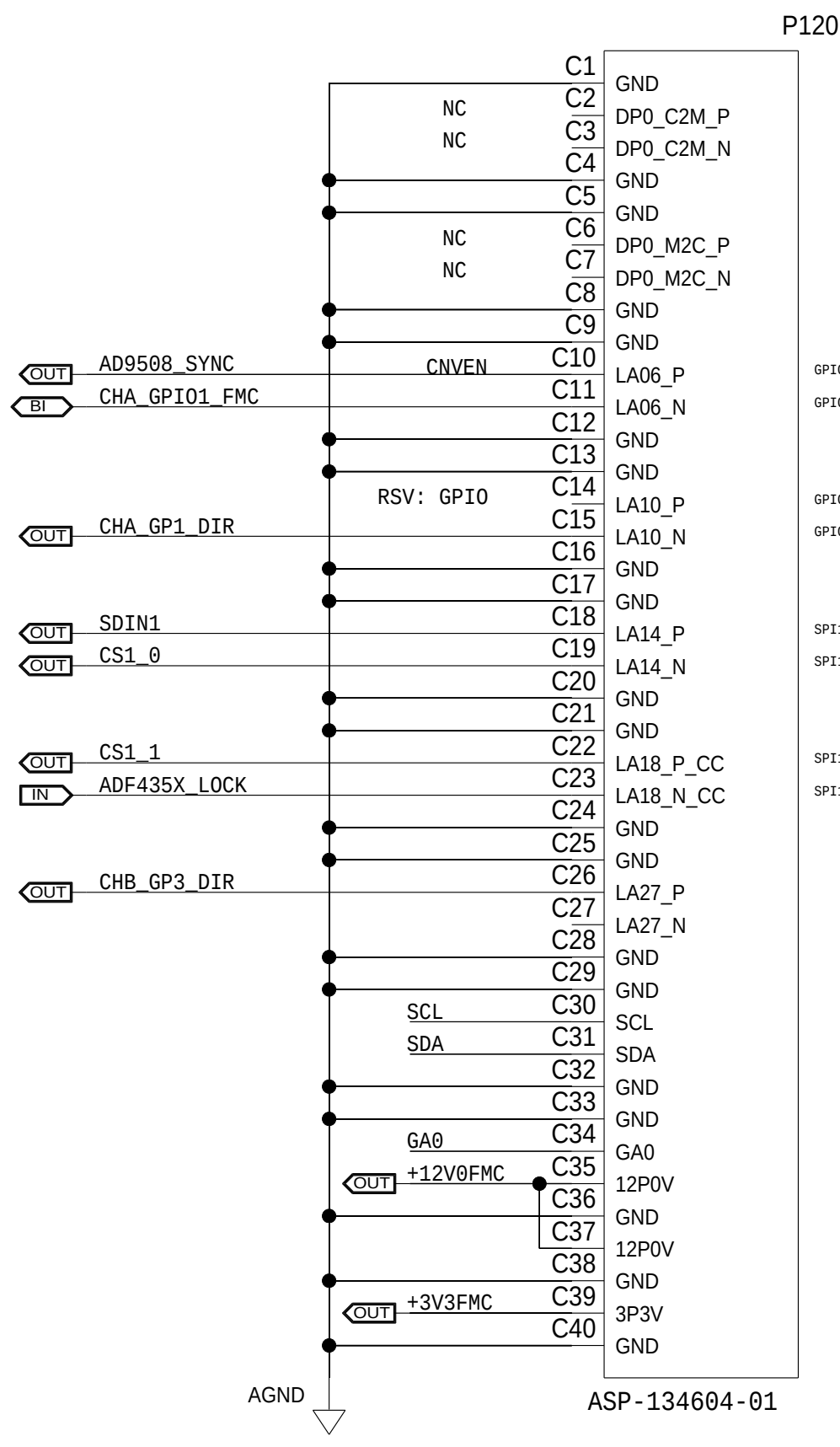
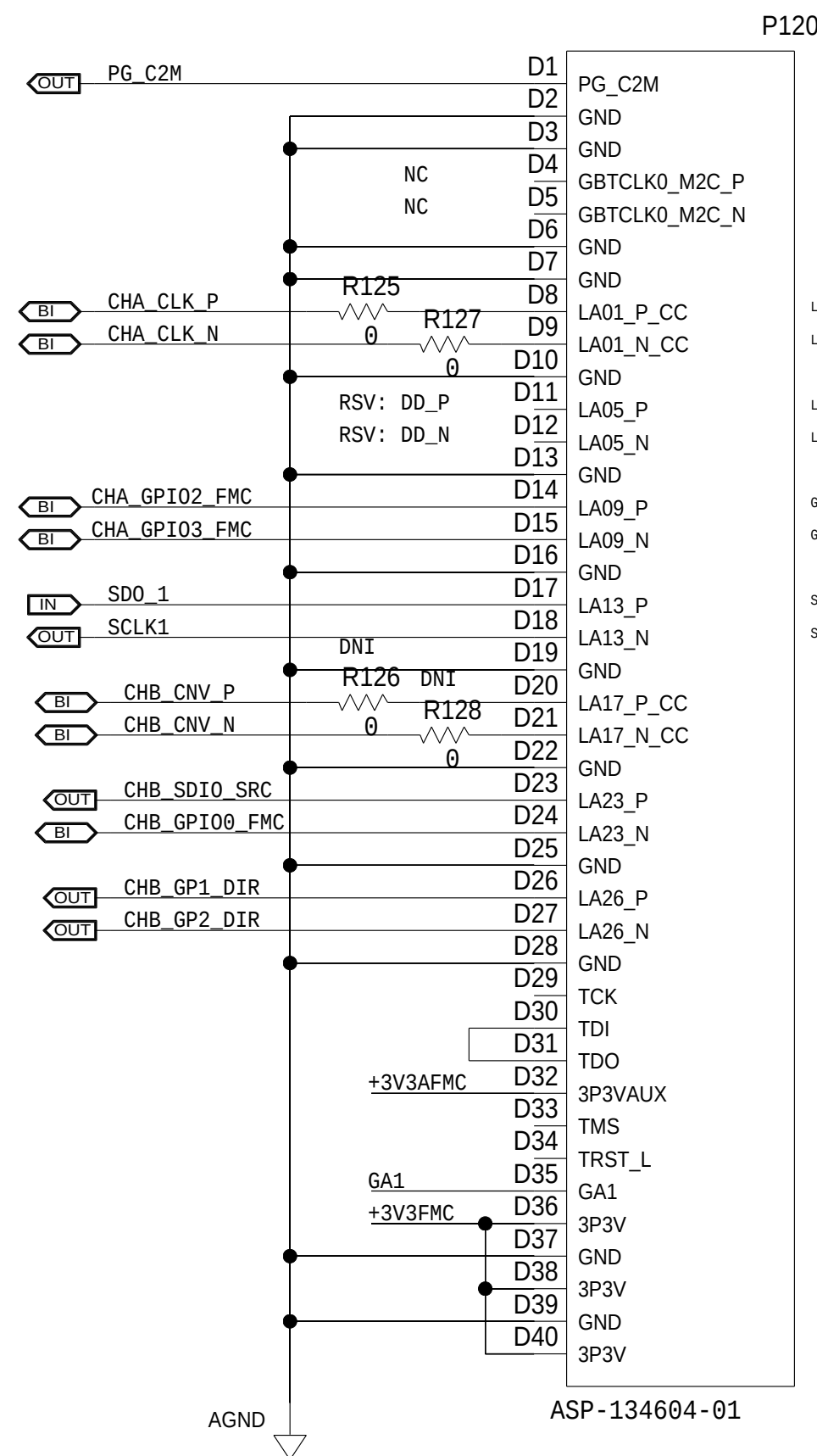
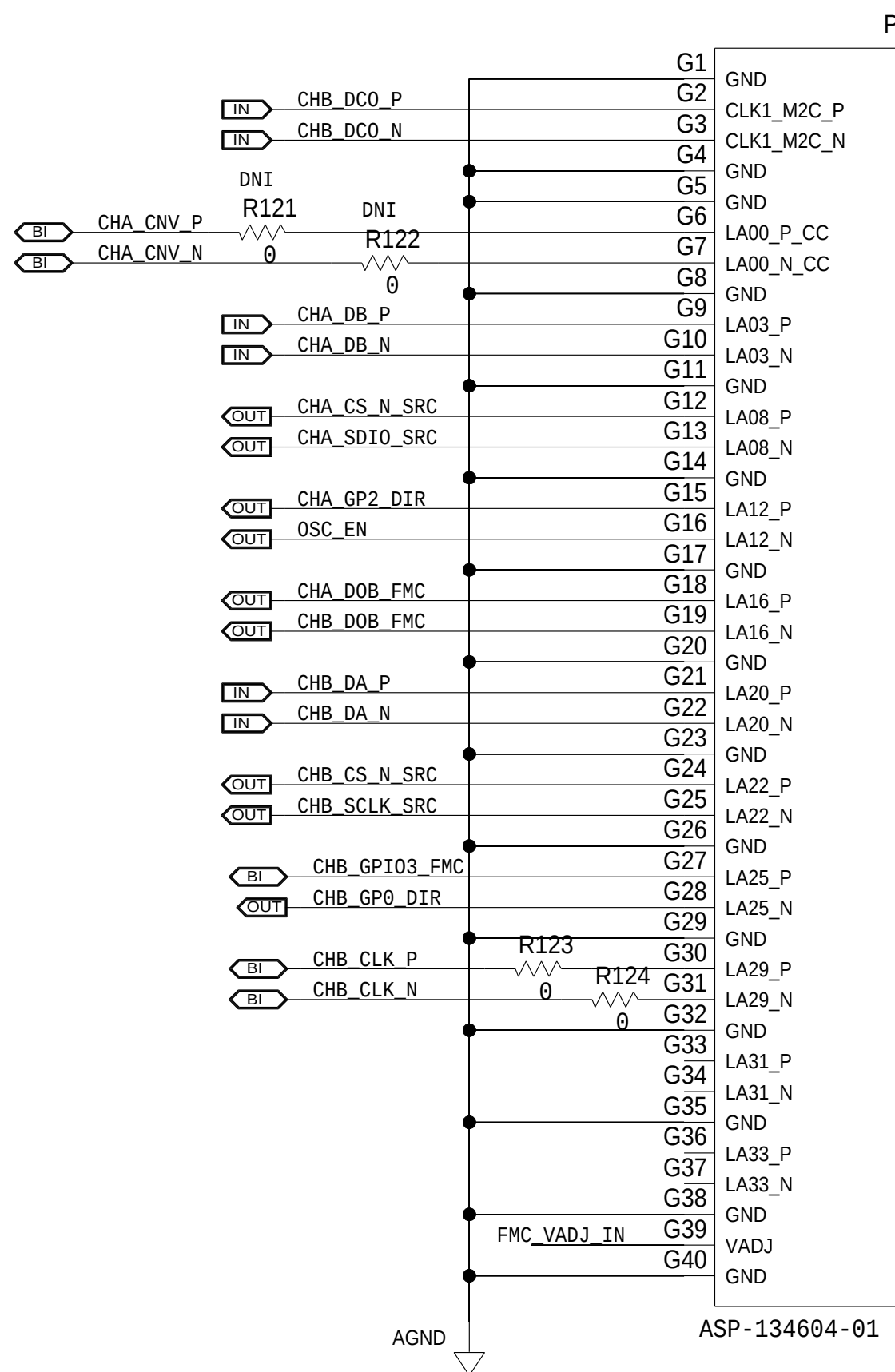
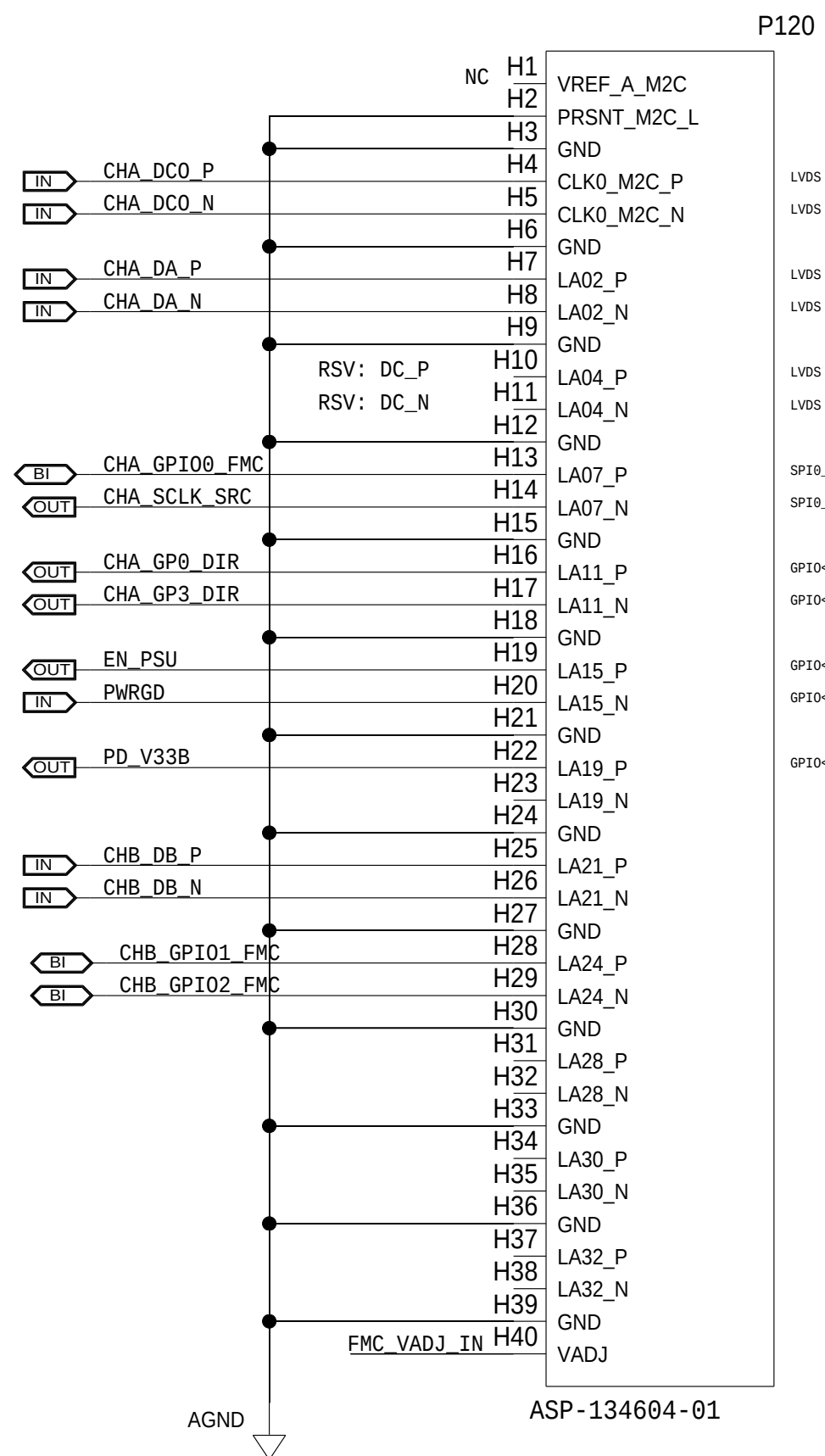
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

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Product(s) : AD4880		REV D	
: AD4883, AD4884, AD4885, AD4886		DESIGN VIEW <DESIGN_VIEW>	
PTD ENGINEER A Jimenez		SIZE D	SCALE 1:1
SHEET 11 OF 12		THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.	

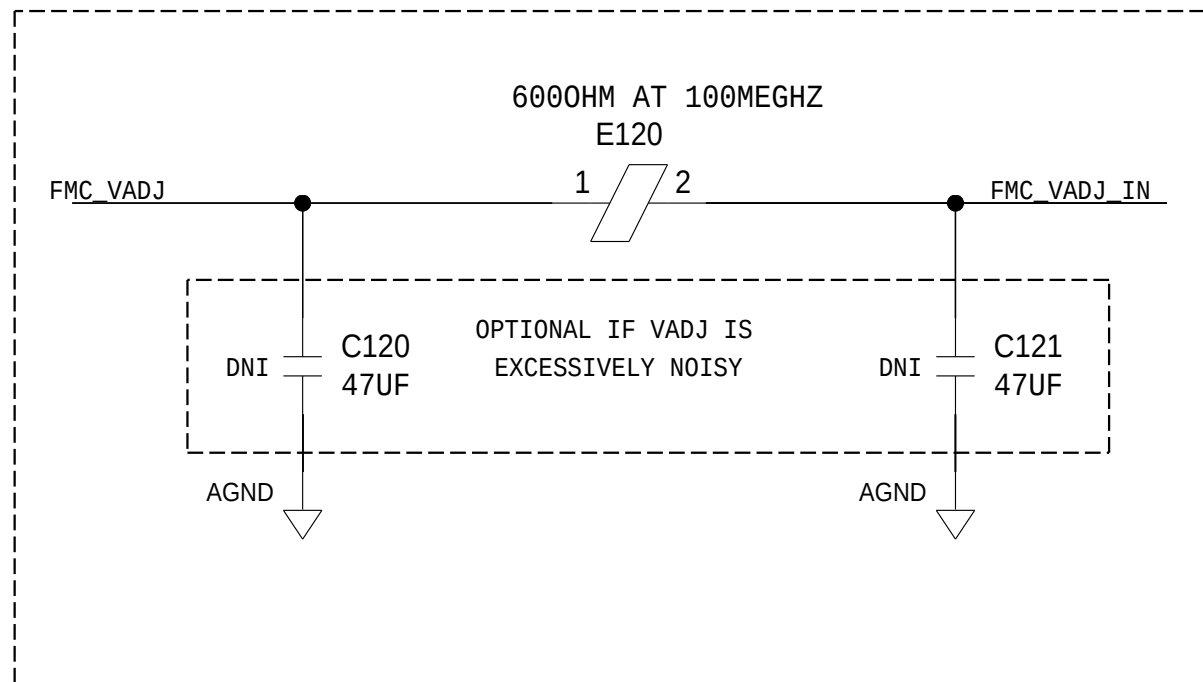
HOST (FMC) INTERFACE

REVISIONS

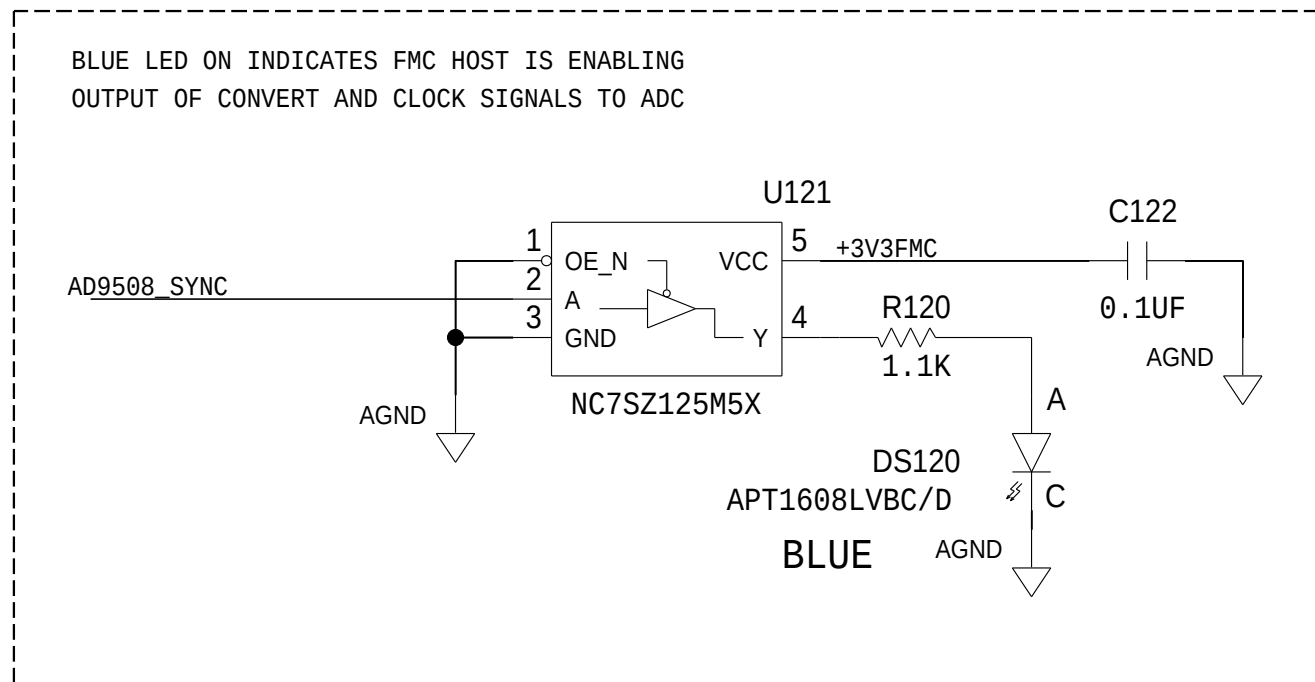
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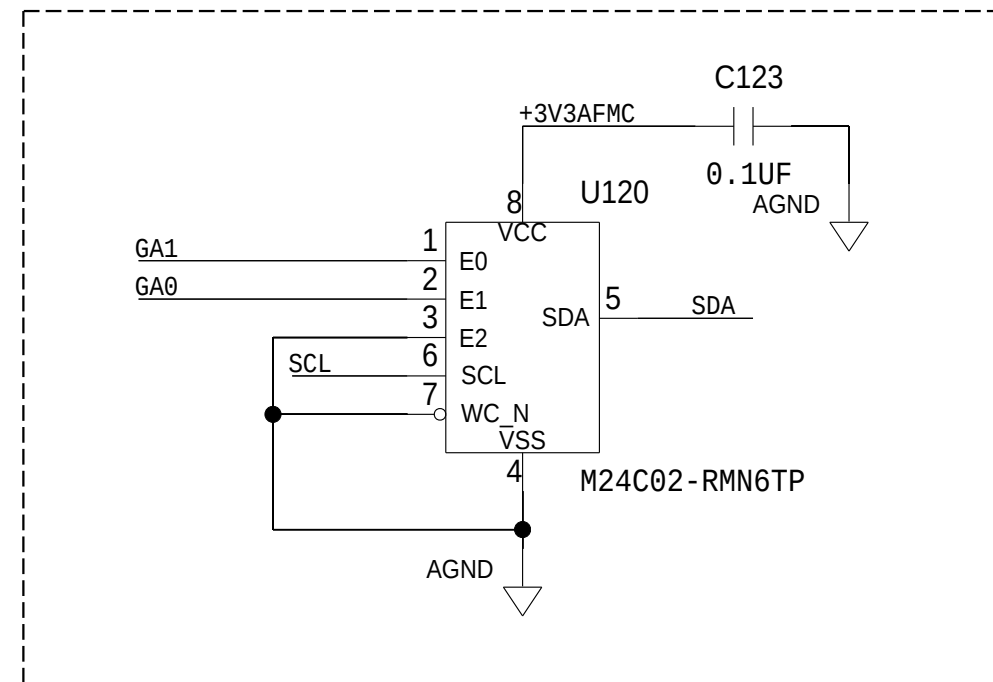
FMC_VADJ RAIL FILTERING



CLOCKING ENABLE LED



BOARD ID EEPROM



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HW TYPE : Customer Evaluation Product(s) : AD4880 : AD4883, AD4884, AD4885, AD4886			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_083437-03	REV D	
PTD ENGINEER A Jimenez	SIZE D	SCALE 1:1	SHEET 12 OF 12